Amendments to the Drawing Figures:

The attached drawing sheet(s) include proposed changes to FIGs. 1-2 and 4-5 and replace(s) the original sheets 1, 3, and 4 including FIGs. 1-2 and 4-5.

Attachment: Replacement Sheet(s)

REMARKS / DISCUSSION OF ISSUES

Claims 1-2, 4-8, and 10-12 are pending in the application; claims 3 and 9 are canceled and claim 12 is newly added herein.

The applicants thank the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority document(s).

Claims are amended for non-statutory reasons: to correct one or more informalities, remove figure label number(s), and/or to replace European-style claim phraseology with American-style claim language.

The Office action objects to the drawings; replacement sheets are attached.

The Office action rejects claims 1-2, 4-8, and 10-11 under 35 U.S.C. 112, second paragraph. The applicants respectfully traverse this rejection. Claims 1, 4, and 10 are correspondingly amended herein. However, the applicants respectfully note that "further functional units" are introduced at line 3 of claim 11, and "a particular one of the further functional units" is introduced at line 5 of claim 11. Withdrawal of this rejection is respectfully requested.

The Office action rejects claims 9 and 11 under 35 U.S.C. 103(a). Claim 9 is canceled herein, and claim 11 is amended to be dependent upon claim 10. Withdrawal of this rejection is respectfully requested.

The Office action rejects claims 1-2 and 5-8 under 35 U.S.C. 103(a) over Rozenshein et al. (USP 6,418,527, hereinafter Rozenshein) and Hennessey et al. ("Computer Organization and Design: The Hardware/Software Interface", hereinafter Hennessey). The applicants respectfully traverse this rejection.

Neither Rozenshein nor Hennessey, individually or collectively, teaches instructions of first and second types, wherein a rate of clocking instruction cycles is varied in dependence upon whether a current segment of program code includes one or more instructions of the second type, as claimed in amended claim 1, upon which claims 2 and 4-8 depend. Accordingly, the applicants respectfully request the Examiner's reconsideration and withdrawal of the rejection of claim 1-2 and 5-8 under 35 U.S.C. 103(a) over Rozenshein and Hennessey.

The Office action rejects claim 10 under 35 U.S.C. 103(a) over Rozenshein and Sager et al. (USP 6,487,675). The applicants respectfully traverse this rejection.

Neither Rozenshein nor Sager, individually or collectively, teaches selecting an instruction cycle rate at which instructions are issued from at least a first and second rate, the first rate being so slow that execution of instructions of the second type by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions of the first type fits within the instruction cycle at the second rate, execution of instructions of the second type not fitting within one instruction cycle at the second rate, as specifically claimed in claim 10, upon which claims 11 and 12 are dependent.

The Office action acknowledges that Rozenshein fails to teach selecting an instruction cycle rate from a first and second rate, and asserts that Sager provides this teaching at column 4, line 48 - column 5, line 6). The applicants respectfully disagree with this assertion.

Sager teaches partitioning a processor into a collection of high-speed latency-intolerant elements, and a collection of lower-speed latency-tolerant elements, and operating each of these partitions at different clock speeds. Sager does not teach selecting an instruction cycle rate for issuing instructions. Within Sagar's processor the two different clock speeds are always provided, all of the elements within the high-speed partition are operated using the high-speed clock, and all of the elements within the lower-speed partition are operated using the low-speed clock.

If Sagar's instruction issuing unit is located within the high-speed partition, instructions will be issued at a high instruction cycle rate; if Sagar's instruction issuing unit is located within the lower-speed partition, instructions will be issued at a low instruction cycle rate. Sager does not teach or suggest alternatively selecting an instruction cycle rate, and specifically teaches that the speed at which any element operates, including the instruction issuing element, is dependent upon where it is placed in the processor. At column 6, lines 26 - column 7, line 20, Sagar suggests, for example, that instruction decoding can be placed in the lower-speed partition:

> "The latency-tolerant execution core 210 includes components which are not latency-sensitive, but which are dependent only upon some level of throughput. In this sense, the latency-tolerant components may be thought of as the "plumbing" whose job is simply to provide a particular "gallons per minute" throughput, in which a "big pipe" is as good as a "fast flow"." (Sagar, column 6, lines 30-36.)
> "We may conclude that the time it takes to decode instructions or rename registers, for example, is significantly less critical than the time it takes to execute instructions." (Sagar, column 7, lines 18-20.)

That is, Sagar teaches that the instructions be issued and decoded at the slower speed, consistent with the intended throughput level, and that the individual elements used to perform the operations required to execute the instructions be operated at the high speed. Sager does not teach that the instructions be issued at different rates, depending upon which type of instruction is to be executed, as taught and claimed by the applicants.

At the text segment cited in the Office action, Sager teaches:

> "FIG. 3 illustrates the high-speed sub-core 205 of the processor 200 of the present invention. The high-speed sub-core includes the most latency-intolerant portions of the particular architecture and/or microarchitecture employed by the processor. For example, in an Intel Architecture processor, certain arithmetic and logic functions, as well as data cache access, may be the most unforgiving of execution latency.
> "Other functions, which are not so sensitive to execution latency, may be contained within a more latency-tolerant execution core 210. For example, in an Intel Architecture processor, execution of infrequently-executed instructions, such as transcendentals, may be relegated to the slower part of the core.

> "The processor 200 communicates with the rest of the system (not shown) via the I/O ring 215. If the I/O ring operates at a different clock frequency than the latency-tolerant execution core, the processor may include a clock mult/div unit 220 which provides clock division or multiplication according to any suitable manner and conventional means. Because the latency-intolerant execution sub-core 205 operates at a higher frequency than the rest of the latency-tolerant execution core 210, there may be a mechanism 225 for providing a different clock frequency to the latency-intolerant execution sub-core 205. In one mode, this is a clock mult/div unit 225." (Sager, column 4, line 48 - column 5, line 6)."

As is clearly evident, the above cited text does not address varying the instruction cycle rate, and cannot be said to support the Office action's assertion that Sager teaches selecting an instruction cycle rate from a first and second rate, as specifically claimed in claim 10.

Further, in KSR Int'l. Co. v. Teleflex, Inc., the Supreme Court noted that the analysis supporting a rejection under 35 U.S.C. 103(a) should be made explicit, and that it is "important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed:

> "Often, it will be necessary ... to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements **in the fashion claimed** by the patent at issue. To facilitate review, this analysis should be made explicit." KSR, 82 USPQ2d 1385 at 1396 (emphasis added).

In support of forming the combination of Rozenshein and Sager, the Office action notes that:

> "The advantage of dividing up the processor functions into a plurality of clock speeds allows for the slower speed function to have a simplified design, which can leasd to decreased chip space usage and power savings. ... Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple clock speeds in the processor of Rozenshein for the advantage of decreased chip space usage and power savings." (Office action, page 17, lines 4-11.)

While these noted advantages of Sager may motivate one of skill in the art to combine Rozenshein and Sager, the applicants respectfully note that these advantages of Sager have no bearing on the applicants' claimed invention. Partitioning a design into high-speed and low-speed areas as taught by Sager can provide advantages in chip space, but providing for a selectable instruction cycle rate as taught by the applicants does not, per se, provide this advantage. Providing a selectable instruction cycle rate does provide power savings advantages, as taught by the applicants, but these advantage are achieved in a different manner than the power savings advantage of Sager's physical partitioning of the processor area.

Even assuming in argument that a combination of Rozenshein and Sager were formed, the applicants respectfully maintain, as detailed above, that such a combination would not result in the applicants' claimed invention. That is, the combination fails to disclose the features of the invention in the fashion claimed, as required by KSR. Accordingly, the applicants respectfully maintain that the rejection of claim 10 under 35 U.S.C. 103(a) over Rozenshein and Sager that relies on Sager for teaching a selectable instruction cycle rate in the fashion claimed in claim 10 is unfounded, and should be withdrawn.

The Office action rejects claim 4 under 35 U.S.C. 103(a) over Rozenshein, Hennessy, Davis (USP 6,367,003), and Sager. The applicants respectfully traverse this rejection.

The combination of Rozenshein, Hennessy, Davis, and Sager fails to disclose a clock circuit that clocks the instruction cycles and includes a plurality of selectable clock rates for clocking the instruction cycles, as specifically claimed in claim 4.

The Office action asserts that Sager teaches a plurality of selectable clock rates for clocking the instruction cycles. As noted above, the applicants respectfully disagree with this assertion, because Sager does not select different clock rates to be applied for issuing instructions. Accordingly, the applicants respectfully maintain that the rejection of claim 4 under 35 U.S.C. 103(a) over Rozenshein, Hennessy, Davis, and Sager that relies on Sager for providing this teaching is unfounded, and should be withdrawn.

In view of the foregoing, the applicants respectfully request that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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